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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,309	02/11/2002	Young-Man Ahn	5649-944	6441

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 06/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/074,309	AHN ET AL.	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-15 and 17-31* is/are rejected.

7)☒ Claim(s) *6 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history* .

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been placed in the file of record.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 7-10, 11 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art ("Admission") in view of Lu et al. (U.S. Pat. No. 5,946,712).

Regarding claims 1, 7-10, 11 and 17-19, Admission in Figs. 1 and 2 discloses an integrated circuit device, comprising: a circuit (including 120) configured to generate an output data signal (ACOUT) in response to a clock signal (OCLK1) and an input data signal (ACIN); a phase-locked loop, clock generation circuit (130) configured to generate the clock signal in response to an input clock signal (CLK); and a plurality of memory devices (M1, M2,..., Mn) configured to respectively receive the output data signal in response to the clock signal, wherein the respective ones of the plurality of memory devices have different respective delays associated therewith with respect to receiving the output data signal (see, for example, instant specification, page 1, lines 12-14 and page 2, lines 18-24).

However, Admission does not disclose a delay circuit configured to delay the clock signal and generate the output data signal in response to the delayed clock signal.

Lu in Figs. 3 and 5 discloses a delay circuit (for example, 160) configured to delay a clock signal (180) and generate an output data signal (output of 158) in response to the delayed clock signal (162).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the circuit of Admission to include the delay circuit of Lu, such that the clock signal is delayed and the output data signal is generated in response to the delayed clock signal, for the purpose of assuring validity of data in a synchronous memory at increased system clock frequencies (see, for example, Lu, column 1, lines 6-10).

4. Claims 2-5, 12-15 and 20-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art ("Admission") in view of Lu et al. (U.S. Pat. No. 5,946,712) as applied to claims 1, 7-10, 11 and 17-19 above, and further in view of Yoshimori (Japanese Patent Pub. No. JP 01161912 A).

Regarding claims 2-5, 12-15 and 20-31, Admission in view of Lu discloses an integrated circuit device and a related method of operating the integrated circuit device as in claims 1, 7-10, 11 and 17-19 above, and further discloses: in Lu, Fig. 5, a delay buffer (within 160) configured to generate a delayed clock signal at an output terminal thereof (output of 186) in response to a delay information (188) and a clock signal received at an input terminal thereof (input for 180), the delay buffer comprising a plurality of buffers (182a-f), a plurality of switches (within 186) that are respectively operable (via 188) to connect selected ones of the plurality of buffers in

series between the input terminal and the output terminal of the delay buffer (one of 184a-d is connected to 162 via a corresponding switch in 186), and a demultiplexer circuit (within 186) configured to generate a plurality of switch control signals (within 186, based on 188), respective ones of the plurality of switches being responsive to the respective ones of the plurality of switch control signals (188 is demultiplexed to operate one of the switches in 186 to connect one of 184a-d to 162); and, in Admission, Fig. 1, that the delay circuit comprises a receiver circuit (register 120) configured to store the input data signal (a function of a register).

However, Admission in view of Lu does not disclose that the delay circuit comprises a memory unit configured to store the delay information therein, and the delay buffer coupled to the memory unit; or a plurality of delay circuits respectively configured to delay a clock signal so as to generate a plurality of output clock signals having differing phases.

Yoshimori in Figs. 1 and 6 discloses a delay circuit comprising a memory unit (5 or 61) configured to store a delay information therein, and a delay buffer (4) coupled to the memory unit and configured to generate a delayed clock signal; and a plurality of delay circuits (2 or 60) respectively configured to delay a clock signal (input to 3 or 63) so as to generate a plurality of output clock signals (output from 4) having differing phases (delay of each of 2 or 60 is controlled individually and independently by a corresponding 5 or 61, respectively), and a respective one of the plurality of delay circuits comprising a memory unit (5 or 61) configured to store a delay information therein, and a delay buffer (4) coupled to the memory unit and configured to generate a delayed clock signal. Yoshimori in Fig. 2 also discloses the delay buffer comprising: a plurality of buffers (23); and a plurality of switches (24) that are

respectively operable to connect selected ones of the plurality of buffers in series between the input terminal and the output terminal of the delay buffer.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the device and the method of Admission in view of Lu to include a plurality of delay circuits, each with a memory unit to store delay information and coupled to a delay buffer (thus, having a delay circuit with a memory unit to store delay information and coupled to a delay buffer), as in Yoshimori, for the purpose of easily and independently adjusting the clock delays and reducing the clock skew.

Allowable Subject Matter

5. Claims 6 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 6 and 16, the prior arts of record do not disclose or suggest an input terminal that is coupled to both a receiver circuit and a memory unit and is configured to receive the input data signal and the delay information therethrough.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Keeth et al. (U.S. Pat. No. 6,026,051) discloses a synchronous memory with a data latch controlled by a delayed clock signal.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (703) 308-1624. The examiner can normally be reached on M-Th 6:00 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (703) 308-2816. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jhh
May 30, 2003

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800